Technical Information Manual

Revision n. 3

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MOD. V 814 series

16 CHANNEL
LOW THRESHOLD
DISCRIMINATORS

NPO:
00101/97:V814x.MUTx/03

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1. General description

1.1. Functional description

The CAEN Model V814 is a 16 CHANNEL LOW THRESHOLD DISCRIMINATOR housed in a single width VME module. The module accepts 16 (either negative or positive) inputs and produces 16 differential ECL outputs with a fan-out of two on four front panel flat cable connectors (a functional block diagram is shown in Fig. 1.2).
Input and output stages are independently organized for each channel. Each channel can be turned on or off via VME by using a mask register (Pattern of Inhibit). The timing stage of the discriminator produces an output pulse whose width is adjustable in a range from 6 to 95 ns via VME.
The discriminator thresholds are individually settable in a range from -1 mV to -255 mV (1 mV step), via VME through an 8-bit DAC, a positive input version (Model V814 P), with the thresholds settable in the 1 mV to 255 mV range, is also available.

VETO and TEST inputs are available on the front panel.

On the front panel a Current Sum output is also available that generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load) ±20 %.

A “MAJORITY” output connector provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value.
The logic OR of discriminator output is available on a front panel connector. The relevant “OR” LED lights up if at least one of the unmasked channels is over threshold.
The module’s operations are completely controlled via software for each channel through the VME bus. The most important are:

- setting the discriminator thresholds (8 bit) from -1 to -255 mV (V814 P: 1÷255 mV).
- setting Pattern of Inhibit; each channel can be turned “ON” or “OFF” by using a mask register.
- setting output width in a range from 6 to 95 ns.
- setting the Majority threshold value.
- common TEST

Several versions of the module are available, please refer to Table 1.1 for details.

Table 1.1:Versions available for the Model V814

Version[1]	Number of channels	PAUX connector[2]	Input type
V814[3]	16	yes	Negative
V814 P[3]	16	yes	Positive
V814 B	16	no	Negative
V814 PB	16	no	Positive

Fig. 1.1: Model type label (example: V814 B)

[1] A label on the printed board soldering side indicates the module's version (see Fig 1.1); all the versions share the same features except where indicated.

[2] The version with the PAUX connector requires the V430 backplane.

[3] Models available exclusively on request.

1.2. Block diagram

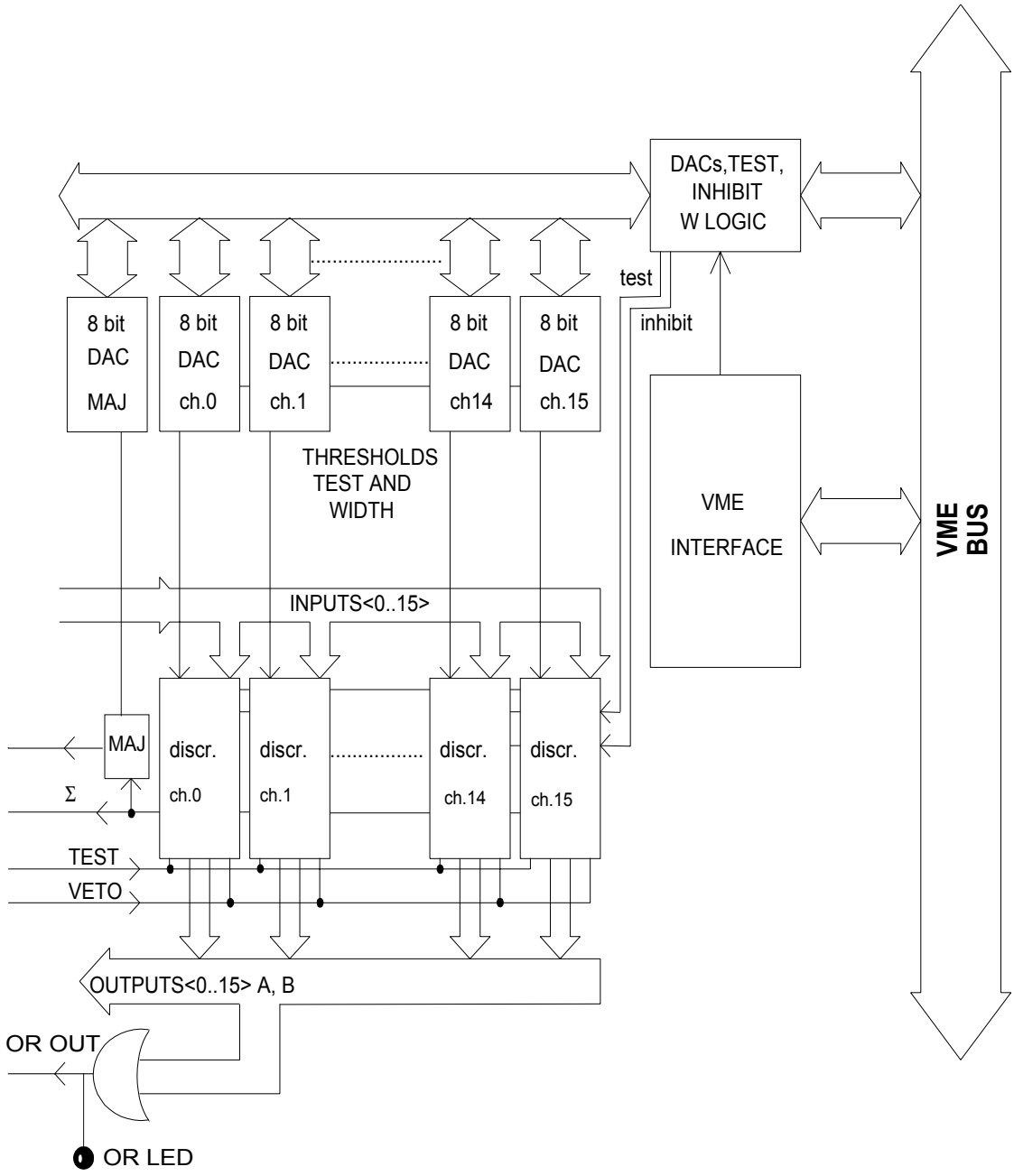


Fig. 1.2: Block Diagram

1.3. Technical specification table

Table 1.2: Technical specification table

Packaging	6U-high, 1U-wide VME unit
Power requirements	Refer to § 2.2
Inputs	16 inputs (50 Ω impedance, DC coupling)
Input voltage range	V814/V814B: -1 mV to -400 mV; V814 P/PB: 1 mV to 400 mV
Max input frequency	60 MHz (8 ns output pulse width)
Double pulse resolution	16 ns (8 ns output pulse width)
Threshold range	V814/V814B: -1 ÷ -255 mV; V814 P/PB: 1 ÷ 255 mV (1 mV step)
Outputs	16 outputs with a fan-out of two (ECL, 110 Ω impedance)
Input/output delay	10.5±1.5 ns
Output width	Programmable from 6±1 ns to 95±7 ns
Interchannel insulation	54 dB for 2.5 ns rise time input signals
Control inputs	NIM logic signals, high impedance: **VETO:** allows vetoing of all channels simultaneously **TEST:** triggers all the enabled channels at once
Control outputs	**MAJORITY:** standard NIM logic signal, 50 Ω impedance; it indicates if the number of input channels over threshold exceeds the MAJORITY level programmed via VME **OR:** standard NIM signal, 50 Ω impedance; logic OR of outputs **Σ:** current proportional to input multiplicity (-1 mA ± 20% per hit), high impedance
Displays	**DTACK:** green LED; lights up at each VME access **OR:** green LED; it lights up if at least one output signal is present

2. Technical Specifications

2.1. Packaging

The modules are housed in 6U-high 1U-wide VME units.
The Mod. V814/V814 P is provided with P1, P2 and PAUX connectors.
The Mod. V814 B/V814 PB is provided with P1, P2 connectors (NO PAUX).

2.2. Power requirements

The power requirements of the various versions are as follows:

Table 2.1: Power requirements

Power supply	V814/V814 P	V814 B/V814 PB (no PAUX)
+ 12 V	100 mA	100 mA
- 12 V	50 mA	50 mA
+ 5 V	800 mA	5.1 A
- 5 V	3.3 A	-

2.3. Front Panel

Fig. 2.1: Mod. V 814 front panel

2.4. External connectors External connectors

The location of the connectors is shown in Fig. 2.1. Their function and electromechanical specifications are listed in the following subsections.

2.4.1. INPUT connectors

INPUT CHANNELS:

Mechanical specifications:
16 LEMO 00 type connectors.
Electrical specifications:
negative polarity, 50 Ohm impedance, DC coupling; ratings: V814: -1÷-400 mV; V814 P: 1÷400 mV; 60 MHz maximum input frequency.

VETO INPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, high impedance, 20 ns minimum FWHM; leading edge of the VETO signal must precede of at least 8 ns the leading edge of the input and overlap completely the input signal; acts on all signals.

TEST INPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, high impedance, 5 ns minimum FWHM, 60 MHz maximum input frequency.

2.4.2. OUTPUT connectors

OUTPUT CHANNELS:

Mechanical specifications:
4 Header 3M 3408-D202 type, 8+8 pin connectors.
Electrical specifications:
Differential ECL level on 110 Ohm impedance; pulse width adjustment from 6±1 ns to 95±7 ns.
Input/Output delay: 10.5±1.5 ns.

OR OUTPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, 50 Ω impedance.

Σ OUTPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
current output (-1 mA ± 20% per hit), high impedance.

MAJORITY OUTPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, 50 Ω impedance.

2.5. Other components

2.5.1. Displays

The front panel hosts the following LEDs:

DTACK
Type: 1 green LED
Function: VME selected; it lights up during a VME access.

OR
Type: 1 green LED
Function: it lights up if at least one output signal is present.

2.5.2. Switches

ROTARY SWITCHES
Function: they allow to select module's VME address; please refer to Fig. 2.2 for their setting.

2.5.3. Jumpers

JP1
Function: it allows to select the Majority logic (Internal, External); please refer to Fig. 2.3 for the jumper location on the V814 board.

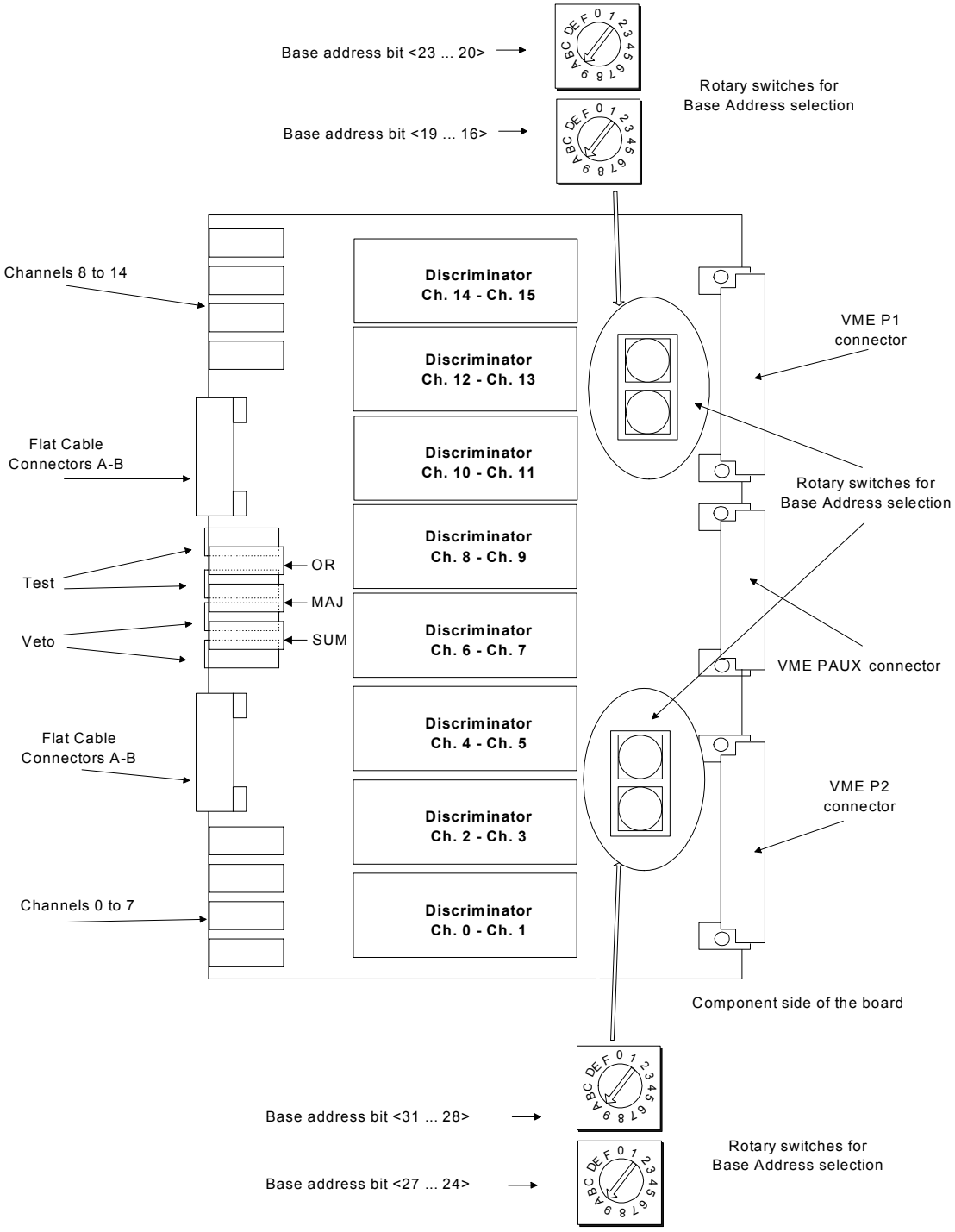


Fig. 2.2: Components location

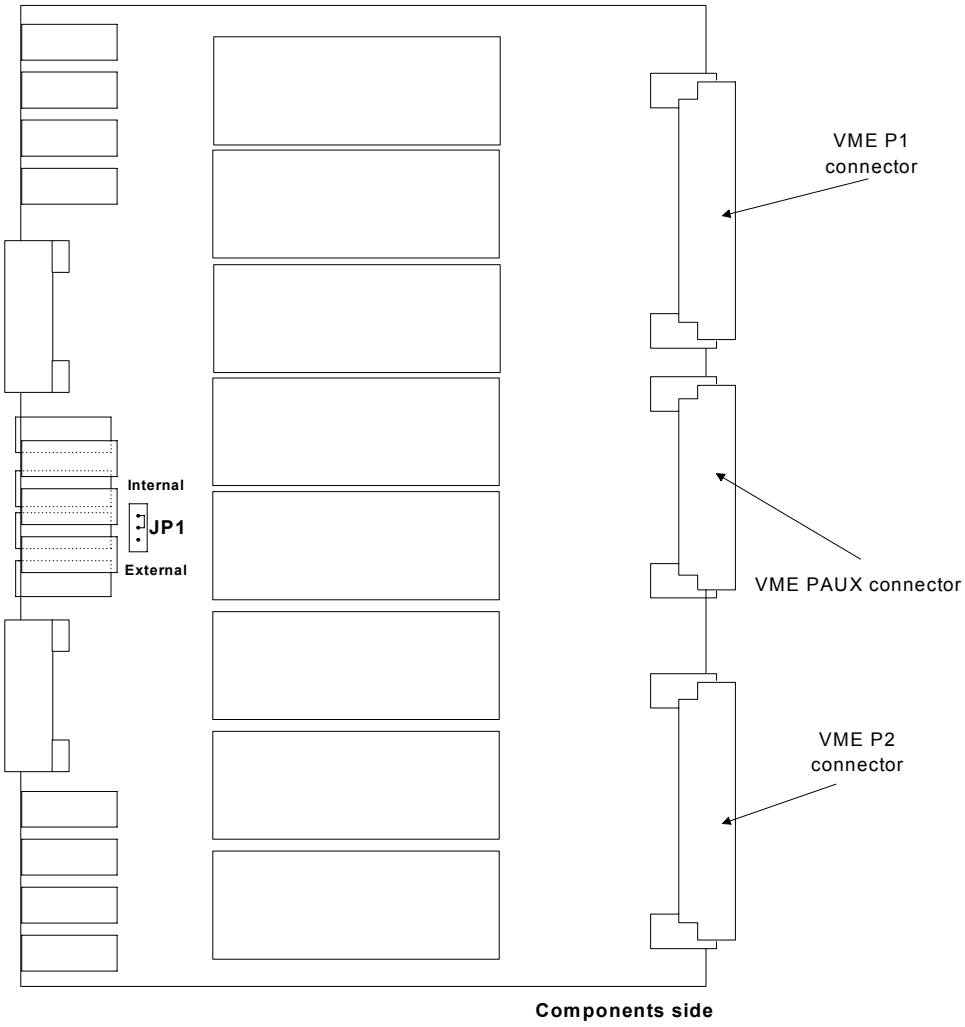


Fig. 2.3: Jumpers location

3. VME Interface

3.1. Addressing capability

The V814 module works in A24/A32 mode. This implies that the module's address must be specified in a field of 24 or 32 bits. The address modifiers codes recognized by the module are:

AM = %39	Standard user data access
AM = %3D	Standard supervisor data access
AM = %09	Extended user data access
AM = %0D	Extended supervisor data access

The module's Base address is fixed by 4 Internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 2.2).
The Base address can be selected in the range:
% 00 0000 <-> % FF 0000 A24 mode
% 0000 0000 <-> % FFFF 0000 A32 mode
The module's address lines A09÷A15 are not connected, so their content is meaningless: for example writing to either Base + 104C or Base + 284C the same register is accessed.

Table 3.1: Address Map

ADDRESS	REGISTER/CONTEN T	TYPE
Base + %00	Threshold register Ch. 0	Write only
Base + %02	Threshold register Ch. 1	Write only
Base + %04	Threshold register Ch. 2	Write only
Base + %06	Threshold register Ch. 3	Write only
Base + %08	Threshold register Ch. 4	Write only
Base + %0A	Threshold register Ch. 5	Write only
Base + %0C	Threshold register Ch. 6	Write only
Base + %0E	Threshold register Ch. 7	Write only
Base + %10	Threshold register Ch. 8	Write only
Base + %12	Threshold register Ch. 9	Write only
Base + %14	Threshold register Ch. 10	Write only
Base + %16	Threshold register Ch. 11	Write only
Base + %18	Threshold register Ch. 12	Write only
Base + %1A	Threshold register Ch. 13	Write only
Base + %1C	Threshold register Ch. 14	Write only
Base + %1E	Threshold register Ch. 15	Write only
Base + %40	Output width register Ch. 0 to 7	Write only
Base + %42	Output width register Ch. 8 to 15	Write only
Base + %48	Majority threshold register	Write only
Base + %4A	Pattern Inhibit register	Write only
Base + %4C	Test pulse register	Write only
Base + %FA	Fixed code	Read only
Base + %FC	Manufacturer & Module type	Read only
Base + %FE	Version & Serial number	Read only

3.2. Geographical address

The board can be addressed via geographical addressing (i.e. according to its position in the crate, neglecting the rotary switches configuration), by specifying address modifier AM=0x2F. Each slot of the VME crate is identified by the status of the SN5...SN1 lines of the JAUX: for example, the slot #5 will have these lines respectively at 00101 and consequently the module inserted in the slot #5 will have a GEO address set to 00101. The geographical address works in A24 mode only. The complete address in A24 mode for geographical addressing is:

A[31:24]	**don't care**
A[23:19]	**GEO**
A[18:16]	**0**
A[15:0]	**offset**

3.3. Discriminator threshold

(Base address + %00 to %1E write only)

These registers contain the discriminator threshold values on 8 bit words. The threshold values can be programmed in a range from -1 mV to -255 mV (Mod. V814 P: 1 to 255 mV) with 1 mV steps, writing an integer number between 0 and 255 into the register; the channel thresholds are individually settable.

3.4. Pattern of Inhibit

(Base address + %4A write only)

This register contains the Pattern of Inhibit, a 16 bit word indicating which channels are either enabled or disabled (bit X=1 $\Rightarrow$ Ch. X enabled…bitX=0 $\Rightarrow$ Ch. X disabled).

3.5. Output width Ch. 0 to 7

(Base address + %40 write only)

This register contains the output pulse width value of the channels 0 through 7 on a 8 bit word. This value can be adjusted in the range from 6 ns to 95 ns, writing an integer number between 0 and 255 into the register. The set value corresponds to the width as follows: 255 leads to a 95 ns pulse duration, 0 leads to a 6 ns pulse duration, with a non-linear relation for intermediate values.

3.6. Output width Ch. 8 to 15

(Base address + %42 write only)

This register contains the output pulse width value of the channels 8 through 15 on a 8 bit word. This value can be adjusted in the range from 6 ns to 95 ns, writing an integer number between 0 and 255 into the register. The set value corresponds to the width as follows: 255 leads to a 95 ns pulse duration, 0 leads to a 6 ns pulse duration, with a non-linear relation for intermediate values.

3.7. Majority threshold

(Base address + %48 write only)

This register allows to set the Majority threshold between 1 and 16 for Internal Majority and between 1 and 20 for External Majority writing a proper value in the Base address + %48 (value range: 1 to 244).
The relation to use is the following

MAJTHR = NINT[(MAJLEV*50 –25)/4],

where NINT is the nearest integer function (allowed values for MAJLEV: 1 to 20) e.g.., if the User wants to use a Majority level of 5, the correct MAJTHR value to use is 56.

3.8. Test pulse

(Base address + %4C write only)

A test pulse on all output channels can be generated by performing a write access at Base address + %4C; the test pulse is generated independently from the number written into this register.

3.9. Module identifier words

(Base address + %FA, + %FC, + %FE, read only)

Three words located at the address Base + %FA, + %FC, + %FE of the page are used to identify the module, as shown in Fig. 3.1:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
Version				Module's serial number												Base + % FE
Manufacturer number						Module type										Base + % FC
%FA Fixed code								%F5 Fixed code								Base + % FA

Fig. 3.1: Module Identifier Words

At the address Base + %FA the two particular bytes allow the automatic localization of the module.
For the Mod. V814 the word at the address Base + %FC has the following configuration:

Manufacturer N° = 000010 b
Type of module = 0001010011

The word located at the address Base + %FE identifies the single module via a serial number, and any change in the hardware (for example the use of faster conversion logic) will be shown by the version number.

4. Principles of operation

4.1. Power ON / Reset status

At power ON the contents of all the module's registers are not determined. A setting of the registers must be performed before any other operation.

4.2. Enabling/Disabling the channels

The User can enable or disable each of the 16 channels via VME by performing a VME write access at Base address + %4A . A channel is enabled if the corresponding bit of the Pattern of Inhibit is high (e. g., bin. 1111 1111 1111 0011, or hex. FFF3, disables channels 2 and 3 of the discriminator).

4.3. Enabling/Disabling the channels

The User can enable or disable each of the 16 channels via VME by performing a VME write access at Base address + %4A. A channel is enabled if the corresponding bit of the Pattern of Inhibit is high (e. g., bin. 1111 1111 1111 0011, or hex FFF3, disables channels 2 and 3 of the discriminator).

4.4. Test, Veto and Or signals

Some operations can be performed by sending two external NIM signals:

- **TEST**: an input signal sent through this connector triggers all the enabled channels at once. This feature allows to test of the module as well as to generate a pattern of pulses suitable to test any following electronics.
- **VETO**: an input signal sent through this connector allows to veto all channels simultaneously. A veto pulse of width T will inhibit the input channels for a period with a T duration. Its leading edge must precede the input signal leading edge by at least 8 ns and overlap completely the input signal.

Note: TEST and VETO are high impedance inputs and each one is provided with two bridged connectors for daisy chaining; the chain has to be terminated on 50 Ohm on the last module; the same is needed also if one module only is used, whose inputs have thus to be properly matched

- An **OR** output connector provides also the logical OR of the output channels. The relevant "OR" LED lights up if at least one of the enabled channels is over threshold.

4.5. Channels test

It is possible to obtain pulses on all channels:

- by sending a NIM pulse through one of the two “TEST” connectors located on the front panel.
- by performing a Write operation at (Base address + %4C).

4.6. Setting the threshold

For each channel of the V814 the discriminator threshold is set up via an 8 bit DAC. The threshold values can be programmed in a range from -1 mV to -255 mV with -1 mV steps (set values: 1 to 255); the V814 P accepts positive pulses, thus the threshold ranges from 1 to 255 mV (step: 1 mV). As in all Constant Fraction Discriminators, these thresholds are to be set above the noise level: they do NOT correspond to the actual level that triggers the discriminator outputs, the latter being a “constant fraction” of the input signals.
In order to write the Threshold for each channel, the User must perform a VME access at (Base address + %00 to %1E).

4.7. Setting the output pulse width

The output pulse width is adjustable on 8 bit from 15 to 250 ns (set values: 0 to 255) and the chosen value is applied to each group of 8 channels each. It can be set at Base address + %40 for channels 0 to 7 and at Base address + %42 for channels 8 to 15. The set value corresponds to the Width as follows: 255 leads to a 250 ns value, 0 leads to a 15 ns value, with a non-linear interpolation for intermediate values.

4.8. Current Sum signal

The front panel also houses the **Current Sum (Σ)** output connector which provides a current proportional to the input signal multiplicity, i.e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load) ±20%.

Note: The **Σ** output requires a 50 Ohm termination for a correct operation of the Majority logic.

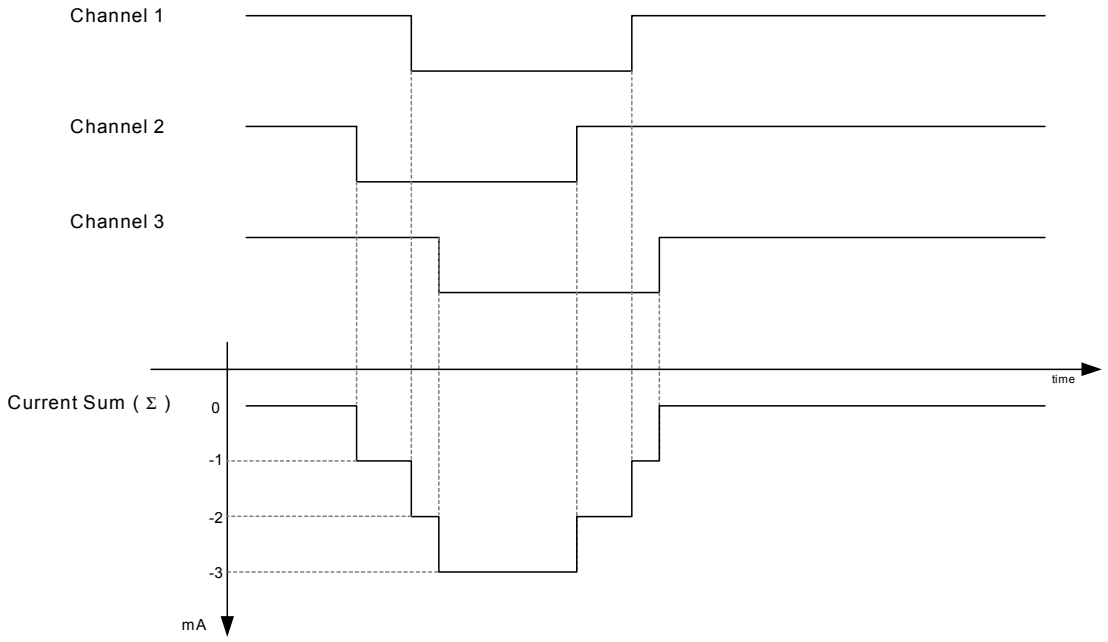


Fig. 4.1: Current Sum signal

4.9. Majority setting

Majority output provides a standard NIM signal if the number of channels over threshold exceeds the programmed majority level (MAJLEV). MAJLEV can be programmed between 1 and 16, writing a proper value (MAJTHR) in the Majority threshold register (see § 3.7); valid values range between 0 and 255. MAJTHR can be calculated in the following way:

MAJTHR = NINT[(MAJLEV*50 – 25)/4]

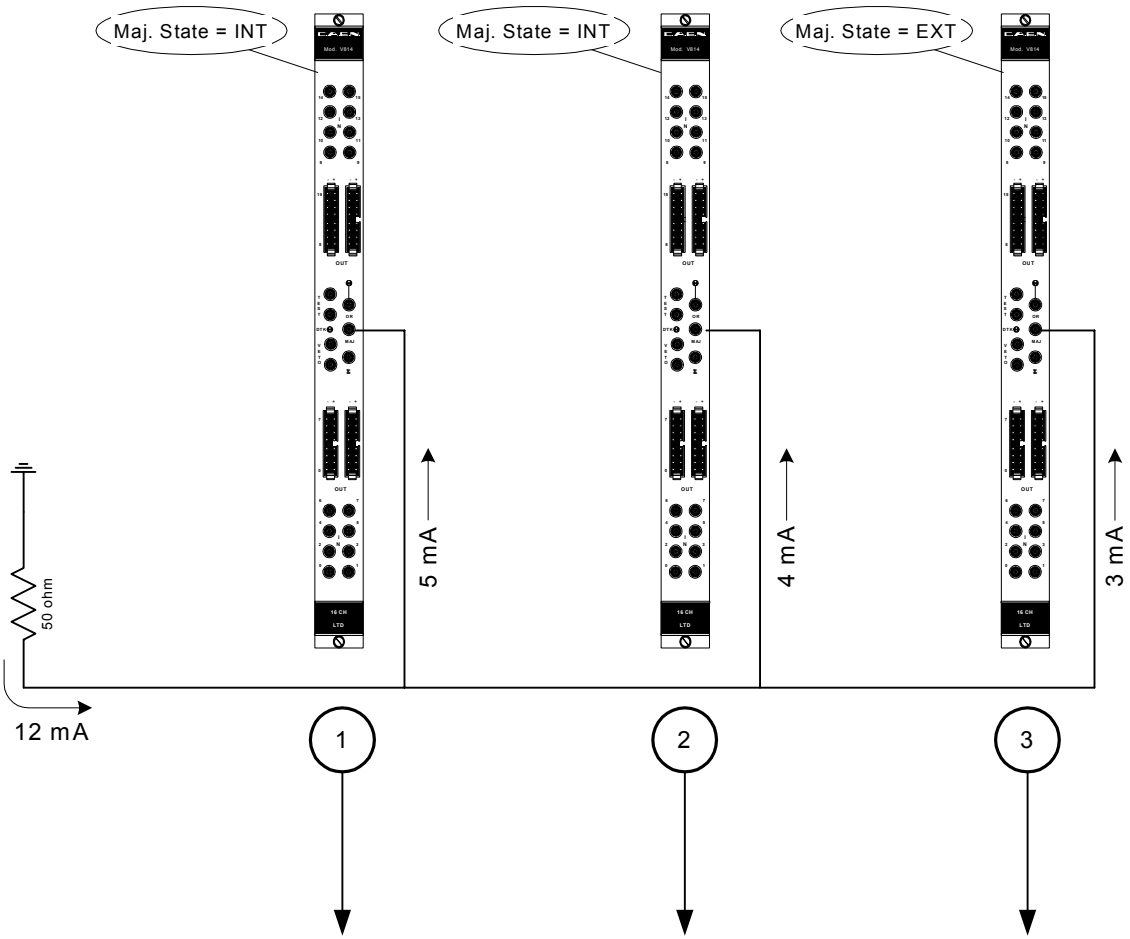
where NINT is the Nearest Integer.

MAJLEV	MAJTHR	MAJLEV	MAJTHR
1	6	11	131
2	19	12	144
3	31	13	156
4	44	14	169
5	56	15	181
6	69	16	194
7	81	17	206
8	94	18	219
9	106	19	231
10	119	20	244

Table 4.1: Majority Level setting values

The Majority logic can be switched from an "Internal" to an "External" position by means of an internal Jumper (see Fig. 2.3).

- **Internal**: With the jumper on the "Internal" position Majority output provides an active signal if the number of the active channels of the module exceeds the programmed majority level (MAJLEV). In this case valid values of MAJLEV are from 1 to 16
- **External**: Several modules can be connected in daisy chain via the Σ outputs. In this case, by setting the Jumper to the "External" position, the Majority logic will act on the sum of the Σ outputs of the connected modules. The majority signal will be active if the sum of chained modules active channels exceeds or is equal to the programmed MAJLEV. (An example with three chained modules is shown in Fig. 4.2). The Σ output line must be terminated with 50 Ohm.



Module Number	1	2	3
Majority State	INT	INT	EXT
Majority Level (MAJLEV)	2 (referred to internal over th. channel)	5 (referred to internal over th. channel)	10 (referred to all chained modules' over th. channels)
Number of Module's active Channels	5	4	3
Majority Output	ACTIVE (5 > MAJLEV)	NON Active (4 < MAJLEV)	ACTIVE (5+4+3 > MAJLEV)

Fig. 4.2: Example of three daisy chained V814